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10/751,440	01/06/2004	Peter Parker Altice JR.	M4065.0993/P993	2571

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EXAMINER	
CHEN, CHIA WEI A	

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,440	ALTICE, PETER PARKER	
	Examiner	Art Unit	
	Chia-Wei A. Chen	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 4, 6, 9, 10-12, 14, 16, 19, 20, 25, 27-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Booth, Jr. (US 6.078,037).

As to claim 1, Booth, Jr. discloses, in Figure 2, a pixel cell (60), comprising:

- a first storage node (36) for storing charge generated at a photosensitive element prior to storing said charge at a floating diffusion region of said pixel cell; and
- a second storage node (46) for storing a portion of said charge generated by said photosensitive element that is not stored by said first storage node (col. 2, lines 48-53).

As to claim 2, Booth, Jr. teaches the pixel cell of claim 1, wherein said photosensitive element is a photodiode (10; col. 2, line 35).

As to claim 4, Booth, Jr. teaches the pixel cell of claim 1, wherein said first storage node comprises a storage capacitor (col. 2, line 48, Fig. 2).

As to claim 6, Booth, Jr. teaches the pixel cell of claim 1, wherein said second storage node comprises a storage capacitor (col. 2, line 48), Fig. 2.

As to claim 9, Booth, Jr. teaches the pixel cell of claim 1 further comprising a first transfer transistor (38) switchably coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 2, lines 54-56).

As to claim 10, Booth, Jr. teaches the pixel cell of claim 1 further comprising:

- a first transfer transistor (38) switchably coupled between said first storage node and said floating diffusion region; and
- a second transfer transistor (48) switchably coupled between said second storage node and said floating diffusion region (col. 2, lines 54-56).

As to claims 11, 12, 14, 16, 19, and 20, these claims only differ from claims 1, 2, 4, 6, 9, and 10 in that claims 11, 12, 14, 16, 19, and 20 claim a semiconductor chip comprising a plurality of pixels (70 of Booth, Jr.), each pixel having the same configuration as claimed in claims 1, 2, 4, 6, 9, and 10. Thus, claims 11, 12, 14, 16, 19, and 20 are analyzed as previously discussed in claims 1, 2, 4, 6, 9, and 10.

As to claim 25, Booth, Jr. teaches a method for operating an image sensor (62), the method comprising:

- receiving, at a first storage node (36) of a pixel cell, charge generated by a photosensitive element of said pixel cell (col. 2, lines 41-49);
- receiving, at a second storage node (46) of said pixel cell, a portion of said charge generated by said photosensitive element not stored at said first storage node (col. 2, lines 41-49); and
- transferring said charge from at least one of said first and second storage nodes to a floating diffusion region (collection node 32) of said pixel cell (col. 2, lines 49-52).

As to claim 27, Booth, Jr. teaches the method of claim 25, wherein said second act of receiving comprises receiving said portion of said charge at a storage capacitor (36) of said pixel cell (col. 2, lines 48-53, Fig. 2).

As to claim 28, Booth, Jr. teaches the method of claim 25, wherein said act of transferring comprises:

- transferring said charge from said first storage node (36) to said floating diffusion region (col. 2, lines 49-52); and
- transferring said charge from said floating diffusion region to a column line associated with said pixel cell (col. 2, lines 50-52). (Bit line serves same purpose as column line.)

As to claim 29, Booth, Jr. teaches the method of claim 25, wherein said act of transferring comprises:

- transferring said charge from said second storage node (46) to said floating diffusion region (col. 2, lines 49-53); and
- transferring said charge from said floating diffusion region to a column line associated with said pixel cell (col. 2, lines 50-52, Fig. 2). (Bit line serves same purpose as column line.)

As to claim 30, Booth, Jr. teaches the method of claim 25, wherein said first act of receiving comprises activating a shutter gate transistor (sampling gate transistor 34) coupled between said first storage node and said photosensitive element (col. 2, lines 46-48, Fig. 2).

As to claim 31, Booth, Jr. teaches the method of claim 25, wherein said second act of receiving comprises activating a shutter gate transistor (sampling gate transistor 44) coupled between said second storage node and said photosensitive element (col. 2, lines 46-48, Fig. 2).

As to claim 32, Booth, Jr. teaches the method of claim 25, wherein said act of transferring comprises activating a transfer transistor (output transistor 38) coupled between at least one of said first and second storage nodes and said floating diffusion region (col. 2, lines 54-56, Fig. 2).

As to claim 33, Booth, Jr. teaches a method for operating an image sensor (62), the method comprising:

- receiving light at a photosensitive element (10)of a first pixel cell;
- transferring charge generated by said photosensitive element to a first storage node (36) of said first pixel cell;
- transferring a portion of said charge not transferred to said first storage node to a second storage node (46) of said first pixel cell;
- transferring said charge from said first storage node to a floating diffusion region (32) of said first pixel cell;
- reading out said charge from said floating diffusion region (col. 2, lines 54-56);
- transferring said charge from said second storage node to said floating diffusion region (42); and
- reading out said charge from said floating diffusion region (col. 2, lines 54-56, col. 2, lines 34-56).

As to claim 34, Booth, Jr. teaches the method of claim 33 further comprising the act of resetting at least one of said photosensitive element and said floating diffusion region (reset transistor 12, col. 2, lines 31-34).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, Jr. (US 6,078,037) in view of Merrill (US 6,069,376).

As to claim 3, Booth, Jr. teaches the pixel cell of claim 1, but does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the pixel of Booth, Jr. to provide a storeage-pixel sensor and an imaging array of storage-pixel sensors that incorporate a "film-speed" switching capability without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 5, Booth Jr. teaches the pixel cell of claim 1 but Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7 of Merrill).

As to claim 7, Booth, Jr. in view of Merrill teaches the pixel cell of claim 3 wherein said gated storage node comprises (86 of Merrill):

- a depletion area (130 of Merrill) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60 of Merrill); and
- a barrier region (126 of Merrill) adjacent to said depletion area (col. 7, lines 54-56 of Merrill).

As to claim 8, Booth, Jr. in view of Merrill teaches the pixel cell of claim 7, wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60 of Merrill).

As to claims 13, 15, 17, and 18, these claims differ only in that these claims claim a semiconductor chip comprising a plurality of pixels (70 of Booth, Jr.), each pixel having the same configuration as claimed in claims 3, 5, 7, and 8. Thus, claims 13, 15, 17, and 18 are analyzed as previously discussed in claims 3, 5, 7, and 8.

As to claim 26, Booth, Jr. teaches the method of claim 25, Merrill teaches wherein said first act of receiving comprises receiving said charge at a gated storage node (86) of said pixel cell (col. 7, line 7 of Merrill).

4. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, Jr. (US 6,078,037) in view of Guidash (US 6,710, 804 B1).

As to claim 21. Booth, Jr. teaches the chip (70) of claim 11, but does not teach the chip further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region.

Guidash teaches the chip further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region (Fig. 1B, col. 3, line 62- col. 4, line 13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have to used the sample and hold circuit of Guidash with the chip of Booth Jr. in order to provide a true correlated double sampling for the photo detector signal level to provide a device that retains provided extended dynamic range while retaining low fixed pattern noise, small pixel, and high sensitivity. (See col. 4, lines 60-61 and col. 2, lines 6-9 of Guidash.)

As to claim 22, Booth, Jr. in view of Guidash teaches the chip of claim 21, wherein said sample and hold circuit comprises at least four storage nodes, each respectively for storing a reset voltage and a signal voltage representing a charge stored by each of said first and second storage nodes (C5 and C6, Fig. 1b of Guidash, col. 4, lines 46-51). (It would have been obvious to one skilled in the art to have used a sample and hold circuit, as taught by Guidash, for each of the storage nodes, as taught in Booth Jr.)

As to claim 23, Booth, Jr. in view of Guidash teaches the chip of claim 21, wherein said sample and hold circuit further comprises at least two storage nodes (C5 and C6 of

Guidash) for respectively storing a reset voltage of said floating diffusion region and a signal voltage of at least one of said first and second storage nodes (col. 4, lines 46-51).

5. Claims 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, Jr. (US 6,078,037) in view of Guidash (US 6,160,281).

As to claim 24, Booth, Jr. teaches a semiconductor chip (70), comprising:

- a plurality of pixel cells comprising:
- a first storage node (36) for storing charge generated at a photosensitive element (10) prior to storing said charge on said common floating diffusion region; and
- a second storage node (46) for storing a portion of said charge generated by said photosensitive element that is not stored by said first storage node (col. 2, lines 48-53);
- but does not teach wherein at least two of which share a common floating diffusion region.

Guidash teaches wherein at least two of which share a common floating diffusion region (84; Fig. 8, col. 4, lines 57-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have have used the common floating diffusion region of Guidash with the semiconductor chip of Booth, Jr. so that layout efficiencies can be utilized to improve the fill factor of the pixel. (See col. 3, lines 1-3 of Guidash (US 6,160,281).)

As to claim 35, Booth, Jr. teaches the method of claim 33 further comprising:

- receiving light at a second photosensitive element (10) of a second pixel cell;
- transferring charge generated by said second photosensitive element to a first storage node (36) of said second pixel cell;
- transferring a portion of said charge not transferred to said first storage node of said second pixel cell to a second storage node (46) of said second pixel cell;
- transferring said charge from said first storage node of said second pixel cell to said floating diffusion region (32);
- reading out said charge from said floating diffusion region (col. 2, lines 54-56);
- transferring said charge from said second storage node of said second pixel cell to said floating diffusion region (42); and
- reading out said charge from said floating diffusion region (col. 2, lines 54-56, col. 2, lines 34-46);

but does not teach wherein said first and second pixel cells share said floating diffusion region.

Guidash teaches wherein said first and second pixel cells share said floating diffusion region (84; Fig. 8, col. 4, lines 57-61).

6. Claims 36, 37, 39, 41, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth Jr. (US 6,078,037) in view of Miyamoto (US 2003/0090575 A1).

As to claims 36, 37, 39, 41, 44, and 45, these claims differ from claims 1, 2, 4, 6, 9, and 10 only in that a processor is additionally recited. Booth Jr. does not teach a processor. Miyamoto teaches a processor (7; paragraph [0029]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the processor of Miyamoto with the system of Booth Jr. to provide an electronic still camera which is capable of effecting continuous shooting at a higher speed, which does not produce a large number of useless exposures during recording, and which is capable of reproducing an image so that the motion of a subject can be easily grasped. (See paragraph [0011] of Miyamoto).

7. Claims 38, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth Jr. (US 6,078,037) in view of Miyamoto (US 2003/0090575 A1) as applied to claim 36 above, and further in view of Merrill (US 6,069,376).

As to claim 38, Booth Jr. in view off Miyamoto does not teach wherein said first storage node comprises a gated storage node.

Merrill teaches wherein said first storage node comprises a gated storage node (86; col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the gated storage node of Merrill with the pixel of Booth, Jr. to provide a storeage-pixel sensor and an imaging array of storage-pixel

sensors that incorporate a "film-speed" switching capability without adding significantly to the layout area of the imaging array. (See col. 2, lines 47-50 of Merrill).

As to claim 40, Booth, Jr. in view of Miyamoto, further in view of Merrill teaches wherein said second storage node comprises a gated storage node (col. 7, line 7 of Merrill).

As to claim 42, Booth, Jr. in view of Miyamoto, further in view of Merrill teaches the processor system of claim 38 wherein said gated storage node comprises (86 of Merrill):

- a depletion area (130 of Merrill) between said photosensitive element and said floating diffusion region (col. 7, lines 58-60 of Merrill); and
- a barrier region (126 of Merrill) adjacent to said depletion area (col. 7, lines 54-56 of Merrill).

As to claim 43, Booth, Jr. in view of Miyamoto, further in view of Merrill teaches the processor system of claim 42, wherein said depletion area and said barrier region comprise oppositely doped silicon (col. 7, lines 54-60 of Merrill).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Krymski (US 2003/0076431 A1) discloses an image sensor with pixels having multiple capacitive storage elements.

Rahn (US 7,170,041 B2) discloses a pixel circuitry for imaging system.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chia-Wei A. Chen whose telephone number is 571-270-1707. The examiner can normally be reached on Monday - Friday, 7:30 - 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cc
8/6/07

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER